CLAIMS

What is claimed is:

1. A programmable driver comprises:

a first driver;

a second driver operably coupled in parallel with the first driver to drive a signal on to a line at a first drive level when a drive control signal is in a first state and wherein, when the drive control signal is in a second state, the second driver is in a high-impedance state such that the first driver drives the signal on to the line at a second drive level, wherein the first drive level is greater than the second drive level; and

controller operably coupled to generate the drive control signal based on load requirements of the line.

2. The programmable driver of claim 1, wherein the first driver further comprises a tri-state driver that is placed in a high impedance state when an output enable signal is in a first state and is placed in an active state when the output enable signal is in a second state.

3. The programmable driver of claim 2, wherein the controller further functions to generate the drive control signal in the second state when the output enable signal is in the first state.

4. The programmable driver of claim 1 further comprises:

a third driver operably coupled in parallel with the first driver to drive the signal on to the line at a third drive level when the drive control signal is in a third state and wherein, when the drive control signal is in the second state, the third driver is in the high-impedance state, wherein the third drive level is greater than the second drive level.

5. The programmable driver of claim 4, wherein the controller further functions to:

generate the drive control signal in a fourth state, wherein, with the drive control signal in the fourth state, the first, second, and third drivers are coupled on parallel to drive the signal on to the line at a fourth drive level, wherein the fourth drive level is greater than the third.

6. The programmable driver of claim 1, wherein the controller further functions to determine the load requirement based on a load impedance on the line or an output signal strength setting.

7. A programmable driver comprises:

a plurality of tri-state drivers; and

controller operably coupled to the plurality of tri-state drivers, wherein, based on a line drive requirement, the controller generates a drive control signal that activates at least one of the plurality of tri-state drivers to drive a signal on to a line at a drive level corresponding to the line drive requirement.

8. The programmable driver of claim 7, wherein each of the plurality of tri-state drivers, when in an active mode, provides an individual drive level.

9. The programmable driver of claim 8, wherein the controller further functions to generate the drive control signal by:

determining a desired drive level based on the line drive requirement;

identifying the at least one of the plurality of tri-state drivers based on the desired drive level and the individual drive levels of each of the plurality of tri-state drivers; and

generating the drive control signal to active the at least one of the plurality of tri-state drivers.

10. The programmable driver of claim 7, wherein the controller comprises a state machine to generate the drive control signal based on the line drive requirement.

11. The programmable driver of claim 7, wherein the controller further functions to generate the drive control signal to place the plurality of tri-state drivers in a high impedance state when an output enable signal is in a first state.

12. The programmable driver of claim 7, wherein the controller further functions to determine the line drive requirement based on a load impedance on the line or an output signal strength setting.

13. A multiple function system on a chip integrated circuit comprises:

a plurality of interface modules operably coupled to receive digital data from a corresponding plurality of external sources;

a digital to analog converter operably coupled to convert digital signals into analog signals;

a processing module;

on-chip memory operably coupled to the processing module, wherein the on-chip memory at least temporarily stores operational instructions that cause the processing module to produce the digital signals from the digital data; and

programmable driver that includes:

a first driver;

a second driver operably coupled in parallel with the first driver to drive the analog signals on to a line at a first drive level when a drive control signal is in a first state and wherein, when the drive control signal is in a second state, the second driver is in a high-impedance state such that the first driver drives the analog signals on to the line at a second drive level, wherein the first drive level is greater than the second drive level; and

controller operably coupled to generate the drive control signal based on load requirements of the line.

14. The multiple function system on a chip integrated circuit of claim 13, wherein the first driver further comprises a tri-state driver that is placed in a high impedance state

when an output enable signal is in a first state and is placed in an active state when the output enable signal is in a second state.

15. The multiple function system on a chip integrated circuit of claim 14, wherein the controller further functions to generate the drive control signal in the second state when the output enable signal is in the first state.

16. The multiple function system on a chip integrated circuit of claim 13, wherein the programmable driver further comprises:

a third driver operably coupled in parallel with the first driver to drive the analog signals on to the line at a third drive level when the drive control signal is in a third state and wherein, when the drive control signal is in the second state, the third driver is in the high-impedance state, wherein the third drive level is greater than the second drive level.

17. The multiple function system on a chip integrated circuit of claim 16, wherein the controller further functions to:

generate the drive control signal in a fourth state, wherein, with the drive control signal in the fourth state, the first, second, and third drivers are coupled on parallel to drive the analog signals on to the line at a fourth drive level, wherein the fourth drive level is greater than the third.

18. The multiple function system on a chip integrated circuit of claim 13, wherein the controller further functions to determine the load requirement based on a load impedance on the line or an output signal strength setting.

19. A multiple function system on a chip integrated circuit comprises:

a plurality of interface modules operably coupled to receive digital data from a corresponding plurality of external sources;

a digital to analog converter operably coupled to convert digital signals into analog signals;

a processing module;

on-chip memory operably coupled to the processing module, wherein the on-chip memory at least temporarily stores operational instructions that cause the processing module to produce the digital signals from the digital data; and

programmable driver that includes:

a plurality of tri-state drivers; and

controller operably coupled to the plurality of tri-state drivers, wherein, based on a line drive requirement, the controller generates a drive control signal that activates at least one of the plurality of tri-state drivers to drive a signal on to a line at a drive level corresponding to the line drive requirement.

20. The multiple function system on a chip integrated circuit of claim 19, wherein each of the plurality of tri-state drivers, when in an active mode, provides an individual drive level.

21. The multiple function system on a chip integrated circuit of claim 20, wherein the controller further functions to generate the drive control signal by:

determining a desired drive level based on the line drive requirement;

identifying the at least one of the plurality of tri-state drivers based on the desired drive level and the individual drive levels of each of the plurality of tri-state drivers; and

generating the drive control signal to active the at least one of the plurality of tri-state drivers.

22. The multiple function system on a chip integrated circuit of claim 19, wherein the controller comprises a state machine to generate the drive control signal based on the line drive requirement.

23. The multiple function system on a chip integrated circuit of claim 19, wherein the controller further functions to generate the drive control signal to place the plurality of tri-state drivers in a high impedance state when an output enable signal is in a first state.

24. The multiple function system on a chip integrated circuit of claim 19, wherein the controller further functions to determine the line drive requirement based on a load impedance on the line or an output signal strength setting.